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128K X25138 16K x 8 Bit

5MHz SPI Serial E²PROM with Block Lock™ Protection

FEATURES

- 5MHz Clock Rate
- Low Power CMOS
  - <1μA Standby Current
  - <5mA Active Current
- 2.5V To 5.5V Power Supply
- SPI Modes (0,0 & 1,1)
- 16K X 8 Bits
  - 32 Byte Page Mode
- Block Lock™ Protection
  - Protect 1/4, 1/2 or all of E²PROM Array
- Programmable Hardware Write Protection
  - In-Circuit Programmable ROM Mode
- Built-in Inadvertent Write Protection
  - Power-Up/Down protection circuitry
  - Write Enable Latch
  - Write Protect Pin
- Self-Timed Write Cycle
  - 5ms Write Cycle Time (Typical)
- High Reliability
  - Endurance: 100,000 cycles
  - Data Retention: 100 Years
  - ESD protection: 2000V on all pins
- Packages
  - 8-Lead XBGA
  - 8, 14-Lead SOIC
  - 8-Lead PDIP
  - 8-Lead TSSOP

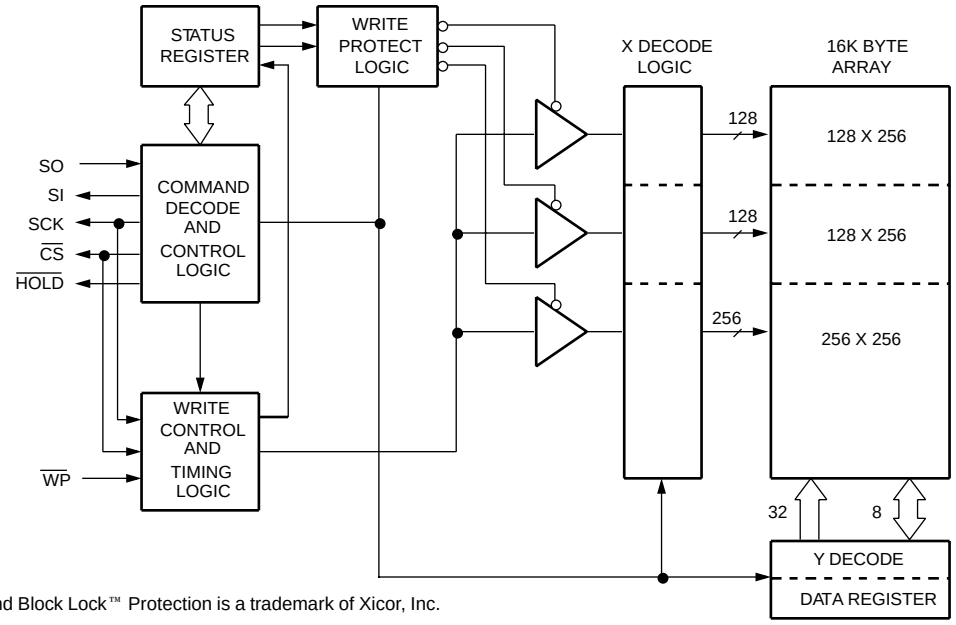
DESCRIPTION

The X25138 is a CMOS 128K-bit serial E²PROM, internally organized as 16K x 8. The X25138 features a Serial Peripheral Interface (SPI) and software protocol allowing operation on a simple three-wire bus. The bus signals are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a chip select ($\overline{CS}$) input, allowing any number of devices to share the same bus.

The X25138 also features two additional inputs that provide the end user with added flexibility. By asserting the $\overline{HOLD}$ input, the X25138 will ignore transitions on its inputs, thus allowing the host to service higher priority interrupts. The $\overline{WP}$ input can be used as a hardwire input to the X25138 disabling all write attempts to the status register, thus providing a mechanism for limiting end user capability of altering 0, 1/4, 1/2 or all of the memory.

The X25138 utilizes Xicor's proprietary Direct Write™ cell, providing a minimum endurance of 100,000 cycles and a minimum data retention of 100 years.

FUNCTIONAL DIAGRAM



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7037 FRM F01

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PIN DESCRIPTIONS

Serial Output (SO)

SO is a push/pull serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

Serial Input (SI)

SI is the serial data input pin. All opcodes, byte addresses, and data to be written to the memory are input on this pin. Data is latched by the rising edge of the serial clock.

Serial Clock (SCK)

The Serial Clock controls the serial bus timing for data input and output. Opcodes, addresses, or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin change after the falling edge of the clock input.

Chip Select ($\overline{CS}$)

When $\overline{CS}$ is HIGH, the X25138 is deselected and the SO output pin is at high impedance and unless an internal write operation is underway, the X25138 will be in the standby power mode. $\overline{CS}$ LOW enables the X25138, placing it in the active power mode. It should be noted that after power-up, a HIGH to LOW transition on $\overline{CS}$ is required prior to the start of any operation.

Write Protect ($\overline{WP}$)

When $\overline{WP}$ is LOW and the nonvolatile bit WPEN is “1”, nonvolatile writes to the X25138 status register are disabled, but the part otherwise functions normally. When $\overline{WP}$ is held HIGH, all functions, including nonvolatile writes operate normally. $\overline{WP}$ going LOW while $\overline{CS}$ is still LOW will interrupt a write to the X25138 status register. If the internal write cycle has already been initiated, $\overline{WP}$ going LOW will have no affect on a write.

The $\overline{WP}$ pin function is blocked when the WPEN bit in the status register is “0”. This allows the user to install the X25138 in a system with $\overline{WP}$ pin grounded and still be able to write to the status register. The $\overline{WP}$ pin functions will be enabled when the WPEN bit is set “1”.

Hold ($\overline{HOLD}$)

$\overline{HOLD}$ is used in conjunction with the $\overline{CS}$ pin to pause the device. Once the part is selected and a serial sequence is underway, $\overline{HOLD}$ may be used to pause

PIN NAMES

Symbol	Description
$\overline{CS}$	Chip Select Input
SO	Serial Output
SI	Serial Input
SCK	Serial Clock Input
$\overline{WP}$	Write Protect Input
V_{SS}	Ground
V_{CC}	Supply Voltage
$\overline{HOLD}$	Hold Input
NC	No Connect

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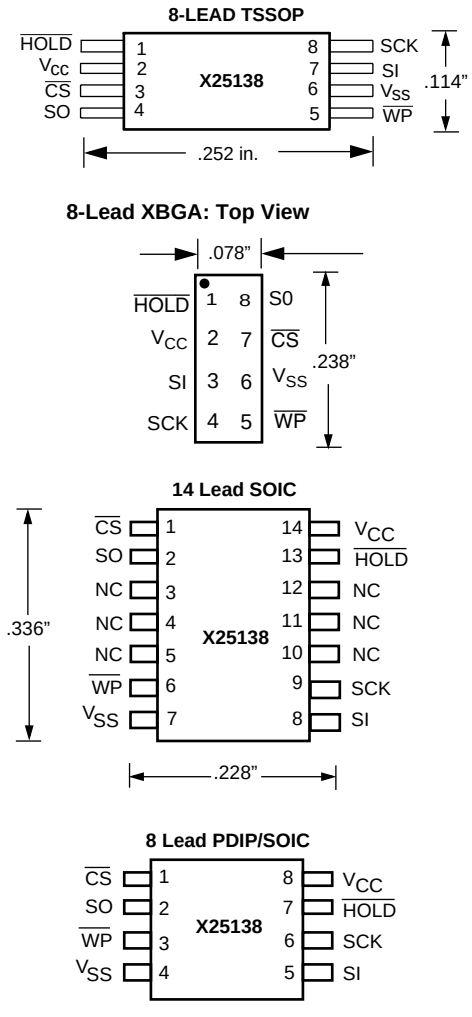
PIN CONFIGURATION



3091 FM 03

the serial communication with the controller without resetting the serial sequence. To pause, $\overline{HOLD}$ must be brought LOW while SCK is LOW. To resume communication, $\overline{HOLD}$ is brought HIGH, again while SCK is LOW. If the pause feature is not used, $\overline{HOLD}$ should be held HIGH at all times.

PRINCIPLES OF OPERATION

The X25138 is a 16K x 8 E^2PROM designed to interface directly with the synchronous serial peripheral interface (SPI) of many popular microcontroller families.

The X25138 contains an 8-bit instruction register. It is accessed via the SI input, with data being clocked in on the rising SCK. $\overline{CS}$ must be LOW and the $\overline{HOLD}$ and $\overline{WP}$ inputs must be HIGH during the entire operation.

Table 1 contains a list of the instructions and their opcodes. All instructions, addresses and data are transferred MSB first.

Data input is sampled on the first rising edge of SCK after $\overline{CS}$ goes LOW. SCK is static, allowing the user to stop the clock and then resume operations. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the $\overline{HOLD}$ input to place the X25138 into a "PAUSE" condition. After releasing $\overline{HOLD}$, the X25138 will resume operation from the point when $\overline{HOLD}$ was first asserted.

Write Enable Latch

The X25138 contains a "write enable" latch. This latch must be SET before a write operation will be completed internally. The WREN instruction will set the latch and the WRDI instruction will reset the latch. This latch is automatically reset upon a power-up condition and after the completion of a byte, page, or status register write cycle.

Status Register

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a write cycle. The status register is formatted as follows:

7	6	5	4	3	2	1	0
WPEN	X	X	X	BL1	BL0	WEL	WIP

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WPEN, BL0 and BL1 are set by the WRSR instruction. WEL and WIP are read-only and automatically set by other operations.

The Write-In-Process (WIP) bit indicates whether the X25138 is busy with a write operation. When set to a "1", a write is in progress, when set to a "0", no write is in progress. During a write, all other bits are set to "1".

The Write Enable Latch (WEL) bit indicates the status of the "write enable" latch. When set to a "1", the latch is set, when set to a "0", the latch is reset.

The Block Lock (BL0 and BL1) bits are nonvolatile and allow the user to select one of four levels of protection. The X25138 is divided into four 32K-bit segments. One, two, or all four of the segments may be protected. That is, the user may read the segments but will be unable to alter (write) data within the selected segments. The partitioning is controlled as illustrated below.

Status Register Bits		Array Addresses Protected
BL1	BL0	
0	0	None
0	1	$3000–$3FFF
1	0	$2000–$3FFF
1	1	$0000–$3FFF

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Table 1. Instruction Set

Instruction Name	Instruction Format*	Operation
WREN	0000 0110	Set the Write Enable Latch (Enable Write Operations)
WRDI	0000 0100	Reset the Write Enable Latch (Disable Write Operations)
RDSR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register
READ	0000 0011	Read Data from Memory Array beginning at selected address
WRITE	0000 0010	Write Data to Memory Array beginning at Selected Address (1 to 32 Bytes)

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*Instructions are shown MSB in leftmost position. Instructions are transferred MSB first.

The Write-Protect-Enable (WPEN) bit is available for the X25138 as a nonvolatile enable bit for the $\overline{WP}$ pin.

WPEN	$\overline{WP}$	WEL	Protected Blocks	Unprotected Blocks	Status Register
0	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	LOW	0	Protected	Protected	Protected
1	LOW	1	Protected	Writable	Protected
X	HIGH	0	Protected	Protected	Protected
X	HIGH	1	Protected	Writable	Writable

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Programmable Hardware Write Protection

The Write Protect ($\overline{WP}$) pin and the nonvolatile Write Protect Enable (WPEN) bit in the Status Register control the Programmable Hardware Write Protect feature. Hardware Write Protection is enabled when $\overline{WP}$ pin is LOW, and the WPEN bit is "1". Hardware Write Protection is disabled when either the $\overline{WP}$ pin is HIGH or the WPEN bit is "0". When the chip is hardware write protected, nonvolatile writes are disabled to the Status Register, including the Block Lock bits and the WPEN bit itself, as well as the block-protected sections in the memory array. Only the sections of the memory array that are not block-protected can be written.

In Circuit Programmable ROM Mode

Note that since the WPEN bit is write protected, it cannot be changed back to a LOW state; so write protection is enabled as long as the WP pin is held LOW. Thus an In Circuit Programmable ROM function can be emplemented by hardwiring the WP pin to Vss, writing to and Block Locking the desired portion of the array to be ROM, and then programming the WPEN bit HIGH. The table above defines the program protect status for each combination of WPEN and WP.

Clock and Data Timing

Data input on the SI line is latched on the rising edge of SCK. Data is output on the SO line by the falling edge of SCK.

Read Sequence

When reading from the E^2PROM memory array, $\overline{CS}$ is first pulled LOW to select the device. The 8-bit READ instruction is transmitted to the X25138, followed by the 16-bit address of which the last 14 are used. After the READ opcode and address are sent, the data stored in the memory at the selected address is shifted out on the SO line. The data stored in memory at the next address can be read sequentially by continuing to provide clock pulses. The address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached ($3FFF) the address counter rolls over to address $0000 allowing the read cycle to be continued indefinitely. The read operation is terminated by taking $\overline{CS}$ HIGH. Refer to the read E^2PROM array operation sequence illustrated in Figure 1.

To read the status register the $\overline{CS}$ line is first pulled LOW to select the device followed by the 8-bit RDSR instruction. After the RDSR opcode is sent, the contents of the status register are shifted out on the SO line. Figure 2 illustrates the read status register sequence.

Write Sequence

Prior to any attempt to write data into the X25138, the "write enable" latch must first be set by issuing the WREN instruction (See Figure 3). $\overline{CS}$ is first taken LOW, then the WREN instruction is clocked into the X25138. After all eight bits of the instruction are transmitted, $\overline{CS}$ must then be taken HIGH. If the user continues the write operation without taking $\overline{CS}$ HIGH after issuing the WREN instruction, the write operation will be ignored.

To write data to the E^2PROM memory array, the user issues the WRITE instruction, followed by the address and then the data to be written. This is minimally a thirty-two clock operation. $\overline{CS}$ must go LOW and remain LOW for the duration of the operation. The host may continue to write up to 32 bytes of data to the X25138. The only restriction is the 32 bytes must reside on the same page. If the address counter reaches the end of the page and the clock continues, the counter will "roll over" to the first address of the page and overwrite any data that may have been written.

For the write operation (byte or page write) to be completed, $\overline{CS}$ can only be brought HIGH after bit 0 of data byte N is clocked in. If it is brought HIGH at any other time the write operation will not be completed. Refer to Figures 4 and 5 below for a detailed illustration of the write sequences and time frames in which $\overline{CS}$ going HIGH are valid.

To write to the status register, the WRSR instruction is followed by the data to be written. Data bits 0, 1, 4, 5 and 6 must be "0". Figure 6 illustrates this sequence.

While the write is in progress following a status register or E^2PROM write sequence, the status register may be read to check the WIP bit. During this time the WIP bit will be HIGH.

Hold Operation

The $\overline{HOLD}$ input should be HIGH (at V_{IH}) under normal operation. If a data transfer is to be interrupted $\overline{HOLD}$ can be pulled LOW to suspend the transfer until it can be resumed. The only restriction is the SCK input must be LOW when $\overline{HOLD}$ is first pulled LOW and SCK must also be LOW when $\overline{HOLD}$ is released.

The $\overline{HOLD}$ input may be tied HIGH either directly to V_{CC} or tied to V_{CC} through a resistor.

Operational Notes

The X25138 powers-up in the following state:

- The device is in the low power standby state.
- A HIGH to LOW transition on $\overline{CS}$ is required to enter an active state and receive an instruction.
- SO pin is high impedance.
- The “write enable” latch is reset.

Data Protection

The following circuitry has been included to prevent inadvertent writes:

- The “write enable” latch is reset upon power-up.
- A WREN instruction must be issued to set the “write enable” latch.
- $\overline{CS}$ must come HIGH at the proper clock count in order to start a write cycle.

Figure 1. Read E^{2}PROM Array Operation Sequence

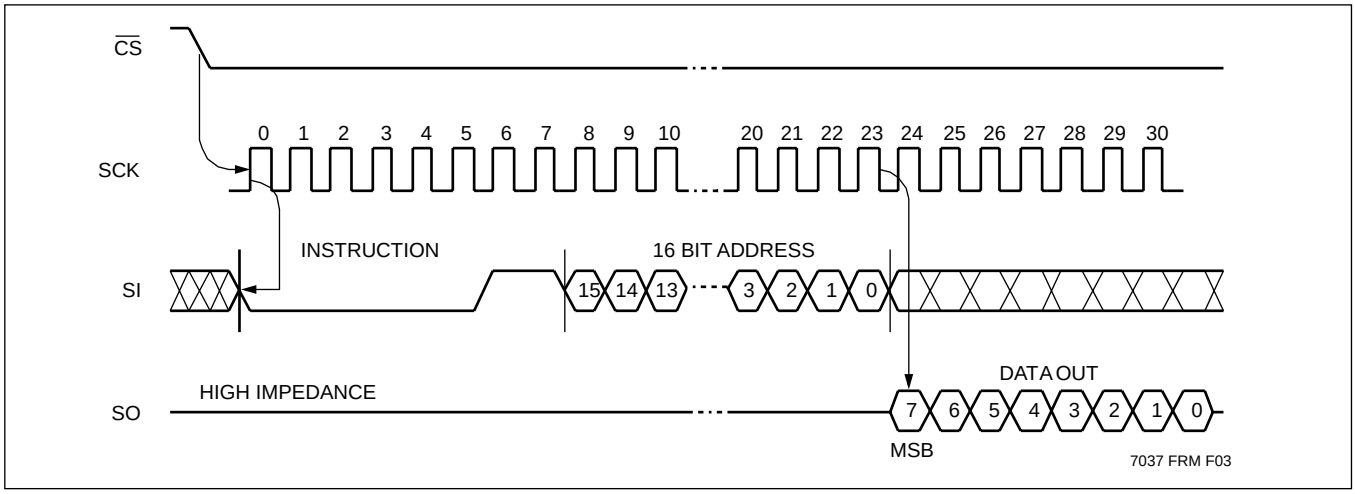


Figure 2. Read Status Register Operation Sequence

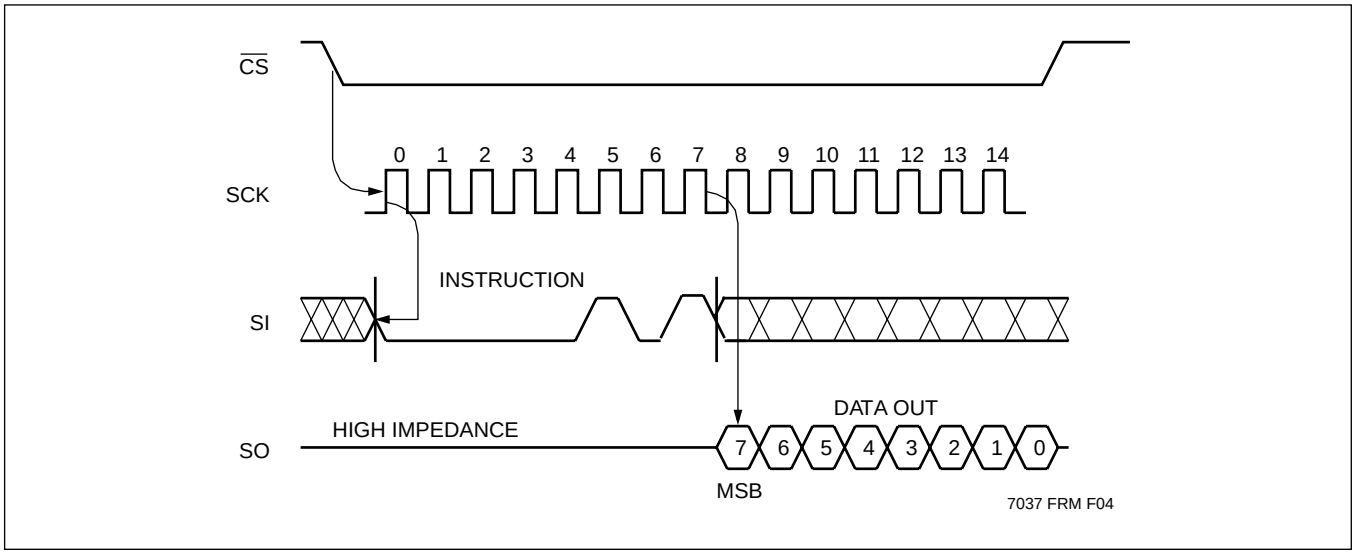


Figure 3. Write Enable Latch Sequence

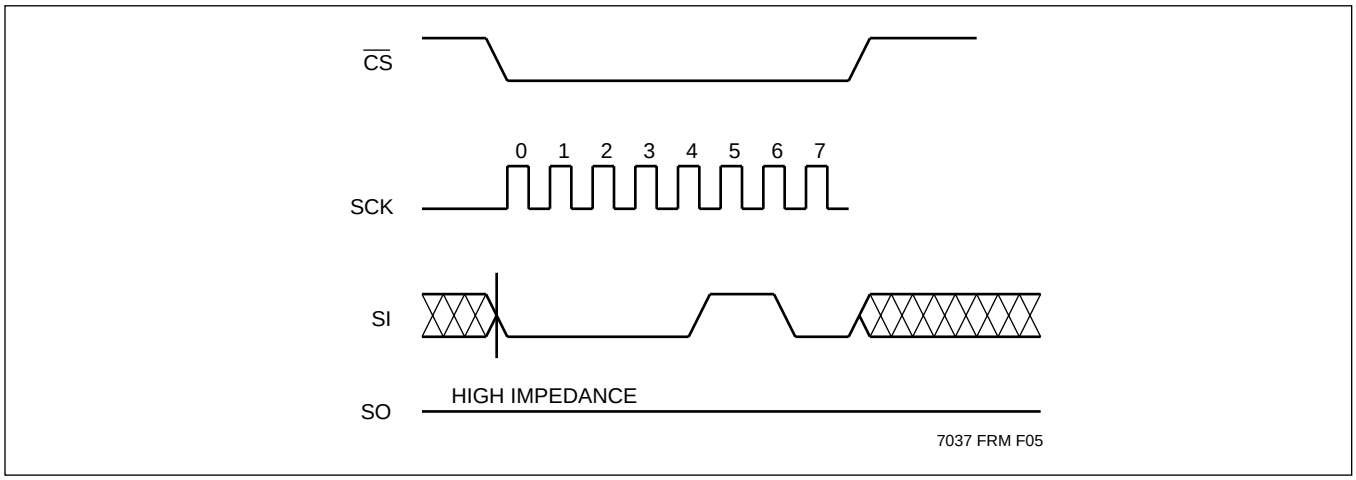


Figure 4. Byte Write Operation Sequence

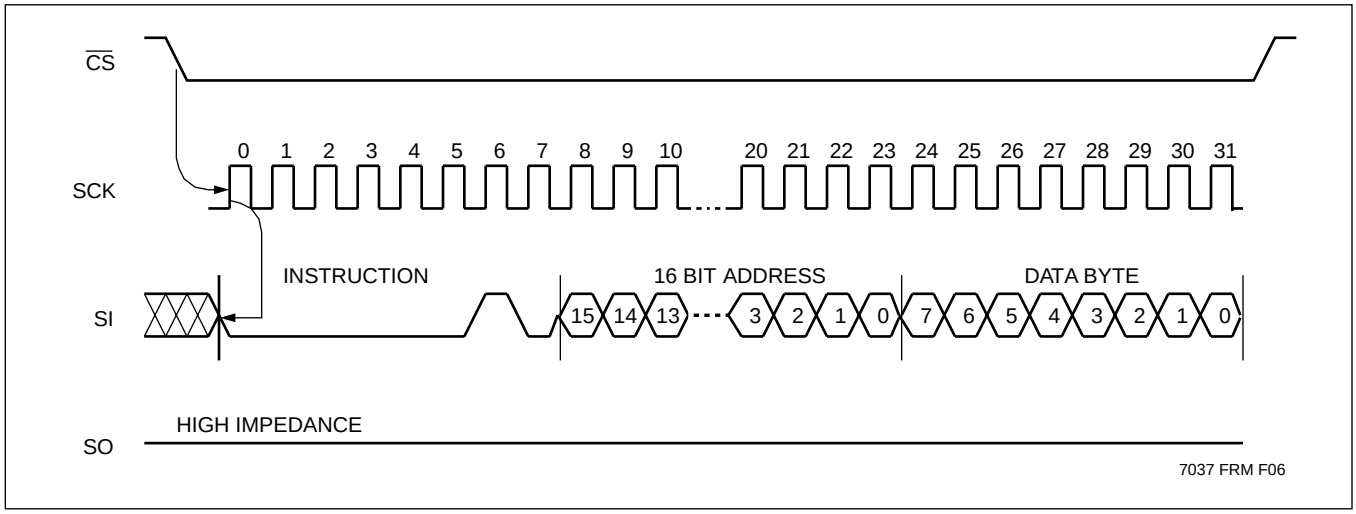


Figure 5. Page Write Operation Sequence

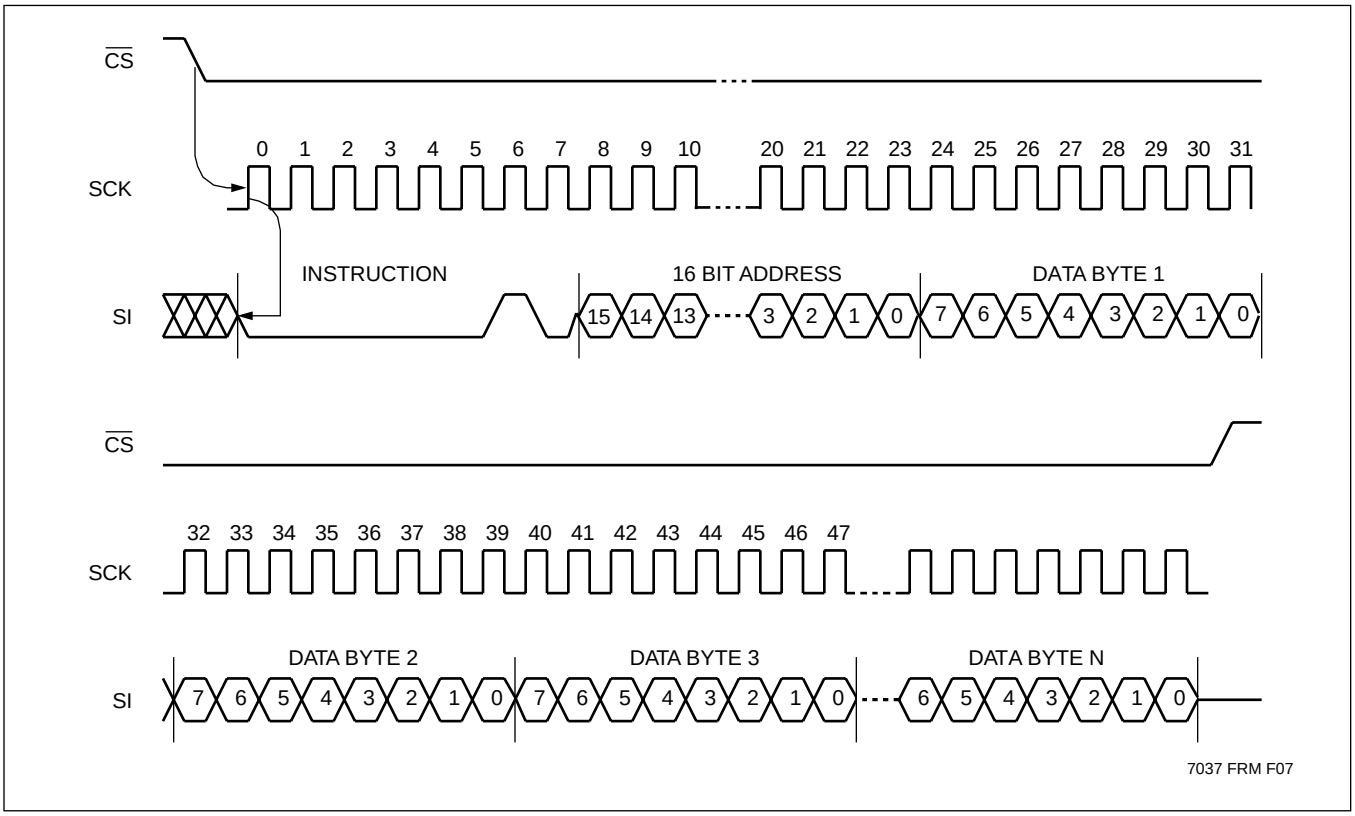
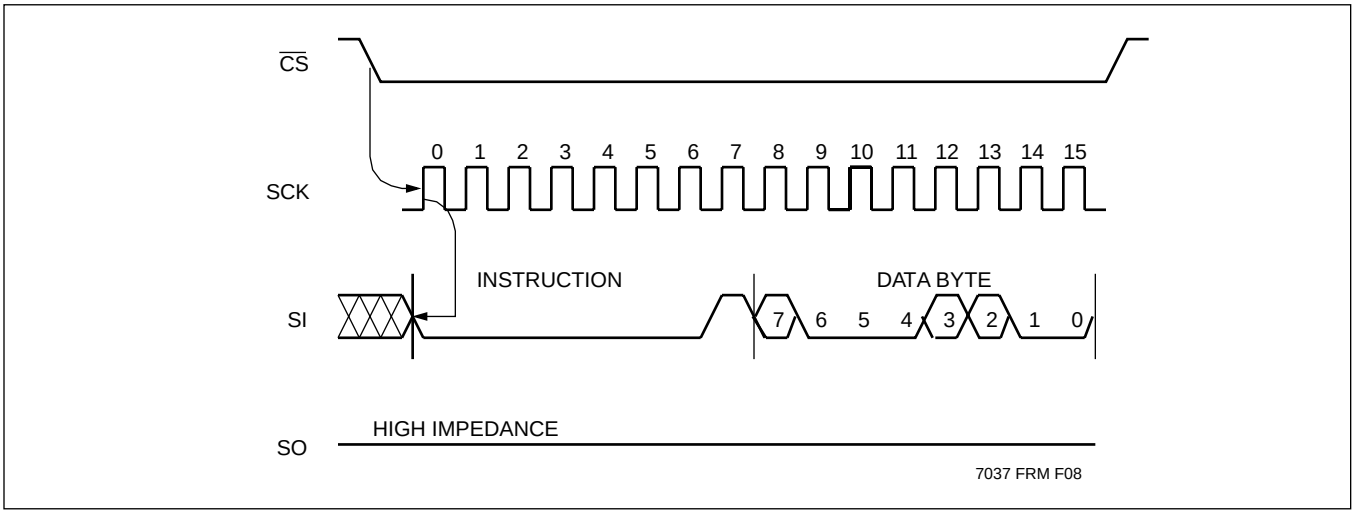


Figure 6. Write Status Register Operation Sequence



ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias.....–65°C to +135°C
Storage Temperature .....–65°C to +150°C
Voltage on any Pin with Respect
to V_{SS} .....–1V to +7V
D.C. Output Current 5mA
(Soldering, 10 seconds) .....300°C

*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

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Supply Voltage	Limits
X25138	5V ±10%
X25138-2.5	2.5V to 5.5V

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D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Supply Current (Active)		5	mA	SCK = V_{CC} x 0.1/V_{CC} x 0.9 @ 5MHz,
I_{SB}	V_{CC} Supply Current (Standby)		1	µA	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC} – 0.3V
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(1)	Input LOW Voltage	–1	V_{CC} x 0.3	V	
V_{IH}(1)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL1}	Output LOW Voltage		0.4	V	I_{OL} = 3mA, V_{CC} = 5V
V_{OH1}	Output HIGH Voltage	V_{CC}–0.8		V	I_{OH} = –1.6mA, V_{CC} = 5V
V_{OL2}	Output LOW Voltage		0.4	V	I_{OL} = 1.5mA, V_{CC} = 3V
V_{OH2}	Output HIGH Voltage	V_{CC}–0.3		V	I_{OH} = –0.4mA, V_{CC} = 3V

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POWER-UP TIMING

Symbol	Parameter	Min.	Max.	Units
T_{PUR}(3)	Power-up to Read Operation		1	ms
T_{PUW}(3)	Power-up to Write Operation		1	ms

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CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$(3)	Output Capacitance (SO)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (SCK, SI, $\overline{CS}$, $\overline{WP}$, $\overline{HOLD}$)	6	pF	V_{IN} = 0V

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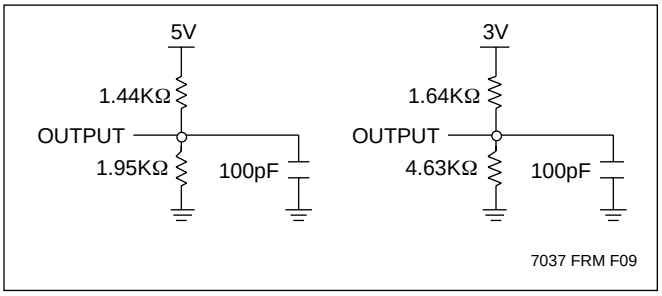
Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.
(3) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT



A.C. CONDITIONS OF TEST

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and OutputTiming Levels	V_{CC} X 0.5

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A.C. OPERATING CHARACTERISTICS

Data Input Timing

Symbol	Parameter	V_{CC} = 2.5V-5.5V		V_{CC} = 4.5V-5.5V		Units
		Min.	Max.	Min.	Max.	
f_{SCK}	Clock Frequency	0	3.3	0	5	MHz
t_{CYC}	Cycle Time	300		200		ns
t_{LEAD}	$\overline{CS}$ Lead Time	150		100		ns
t_{LAG}	$\overline{CS}$ Lag Time	150		100		ns
t_{WH}	Clock HIGH Time	130		80		ns
t_{WL}	Clock LOW Time	130		80		ns
t_{SU}	Data Setup Time	30		20		ns
t_H	Data Hold Time	30		20		ns
t_{RI}(4)	Data In Rise Time		2		2	µs
t_{FI}(4)	Data In Fall Time		2		2	µs
t_{HD}	$\overline{HOLD}$ Setup Time	60		40		ns
t_{CD}	$\overline{HOLD}$ Hold Time	60		40		ns
t_{CS}	$\overline{CS}$ Deselect Time	100		100		ns
t_{WC}(5)	Write Cycle Time		10		10	ms

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Data Output Timing

Symbol	Parameter	V_{CC} = 2.5V-5.5V		V_{CC} = 4.5V-5.5V		Units
		Min.	Max.	Min.	Max.	
f_{SCK}	Clock Frequency	0	3.3	0	5	MHz
t_{DIS}	Output Disable Time		150		100	ns
t_V	Output Valid from Clock LOW		130		80	ns
t_{HO}	Output Hold Time	0		0		ns
t_{RO}(4)	Output Rise Time		50		50	ns
t_{FO}(4)	Output Fall Time		50		50	ns
t_{LZ}(4)	$\overline{HOLD}$ HIGH to Output in Low Z	50		50		ns
t_{HZ}(4)	$\overline{HOLD}$ LOW to Output in High Z	50		50		ns

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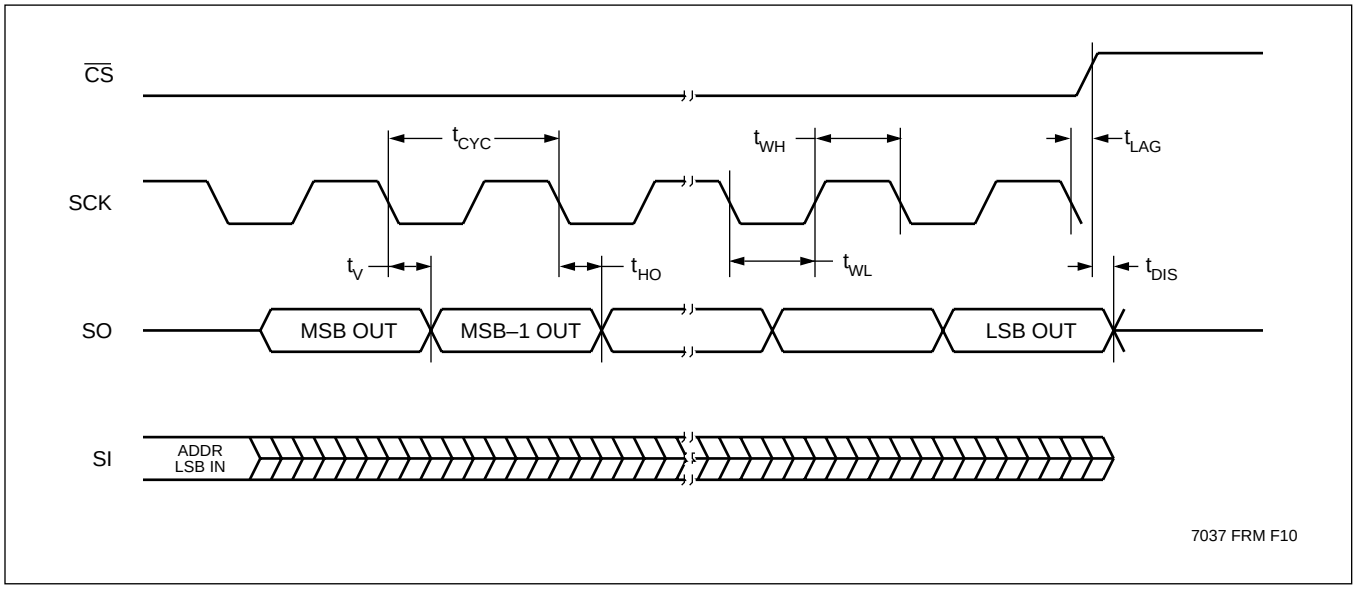
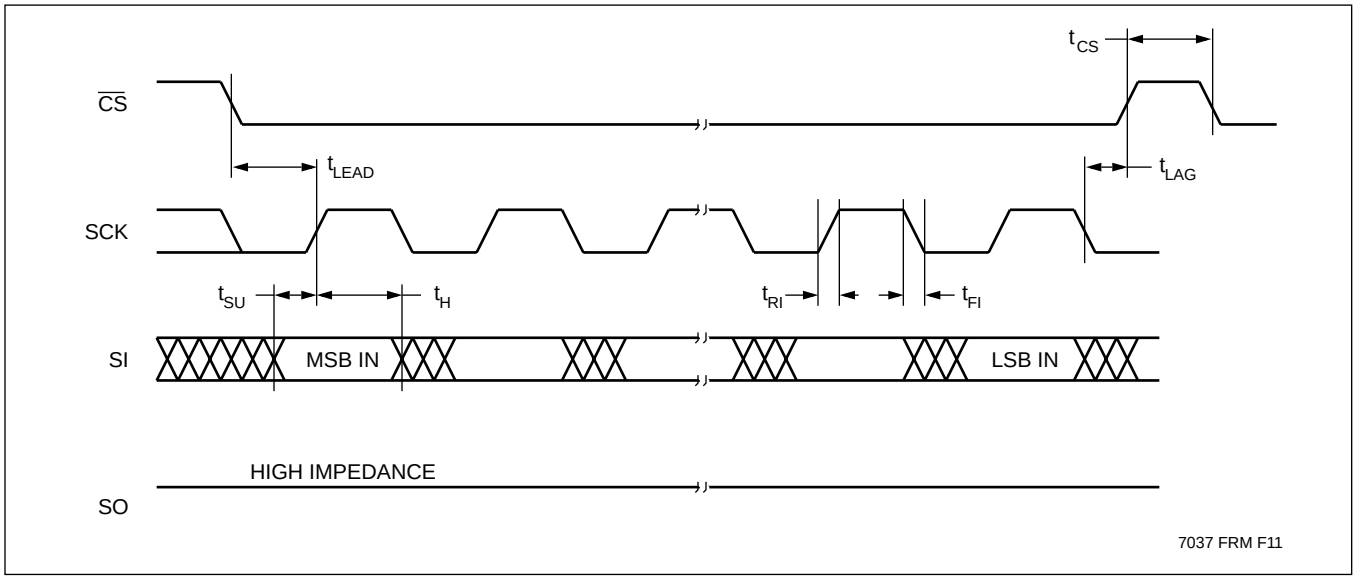
Notes: (4) This parameter is periodically sampled and not 100% tested.

(5) t_{WC} is the time from the rising edge of $\overline{CS}$ after a valid write sequence has been sent to the end of the self-timed internal nonvolatile write cycle

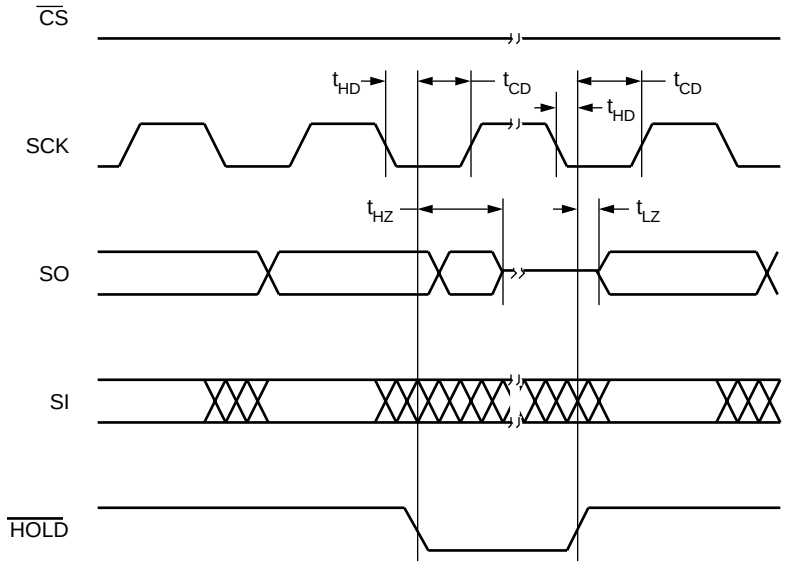
Serial Output Timing



Serial Input Timing

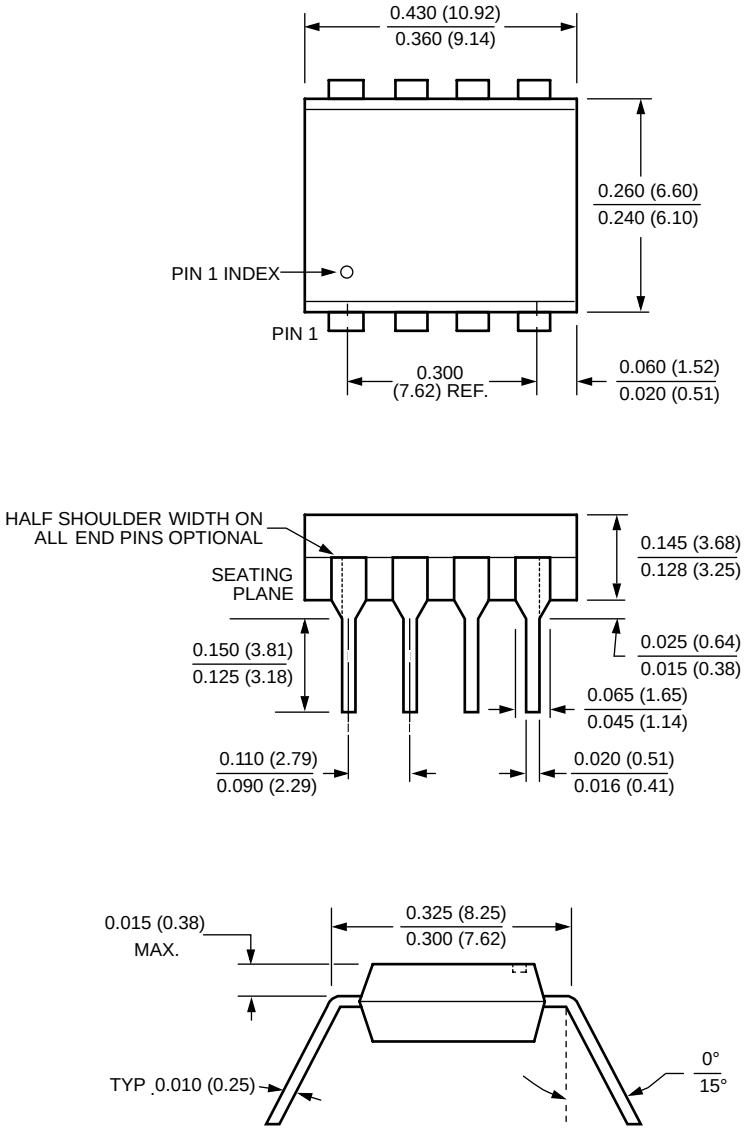


Hold Timing



PACKAGING INFORMATION

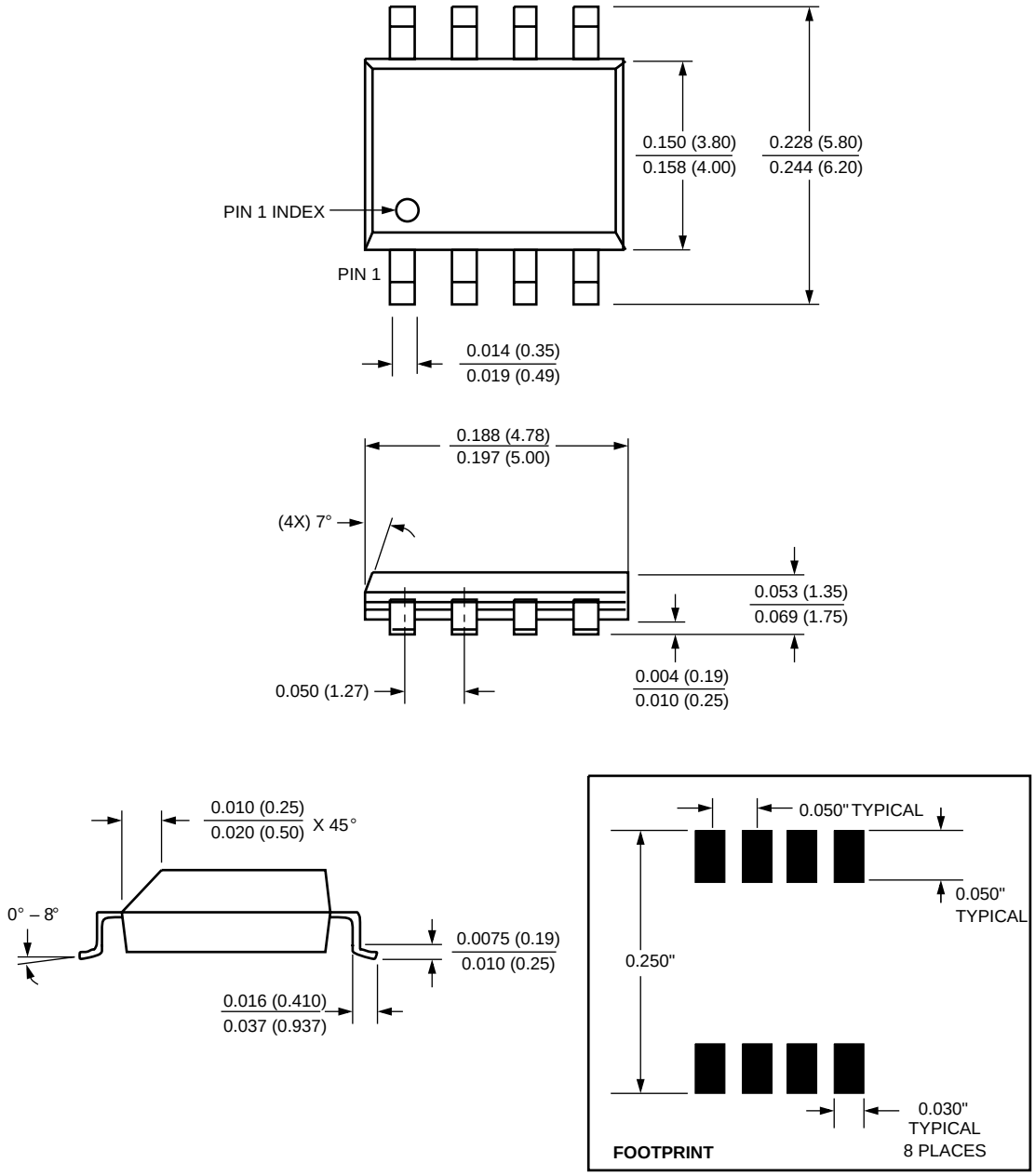
8-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



NOTE:

1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH**

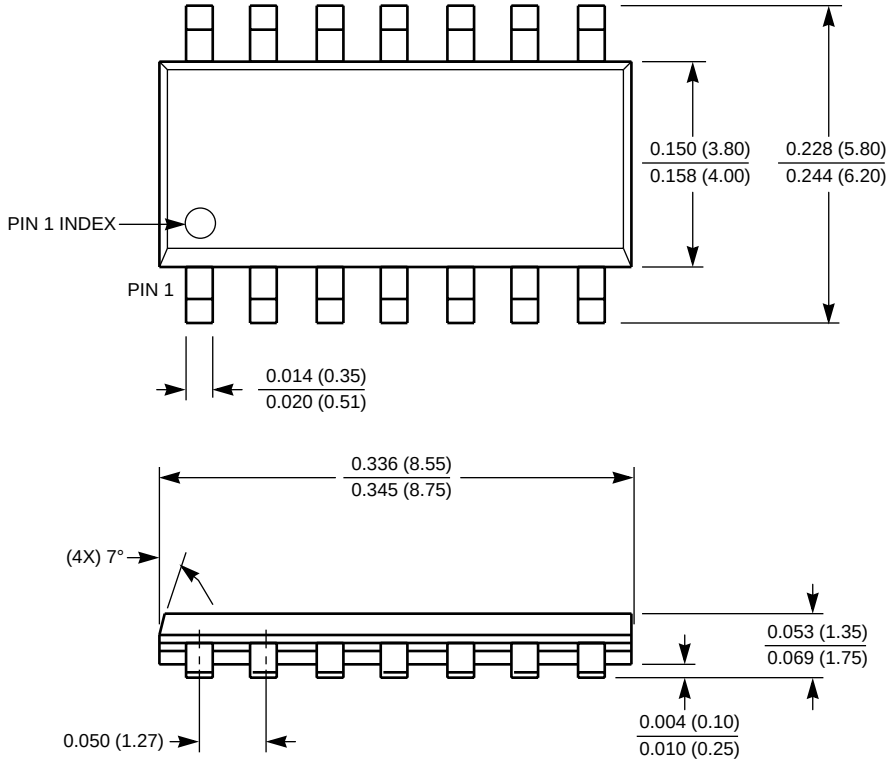
8-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

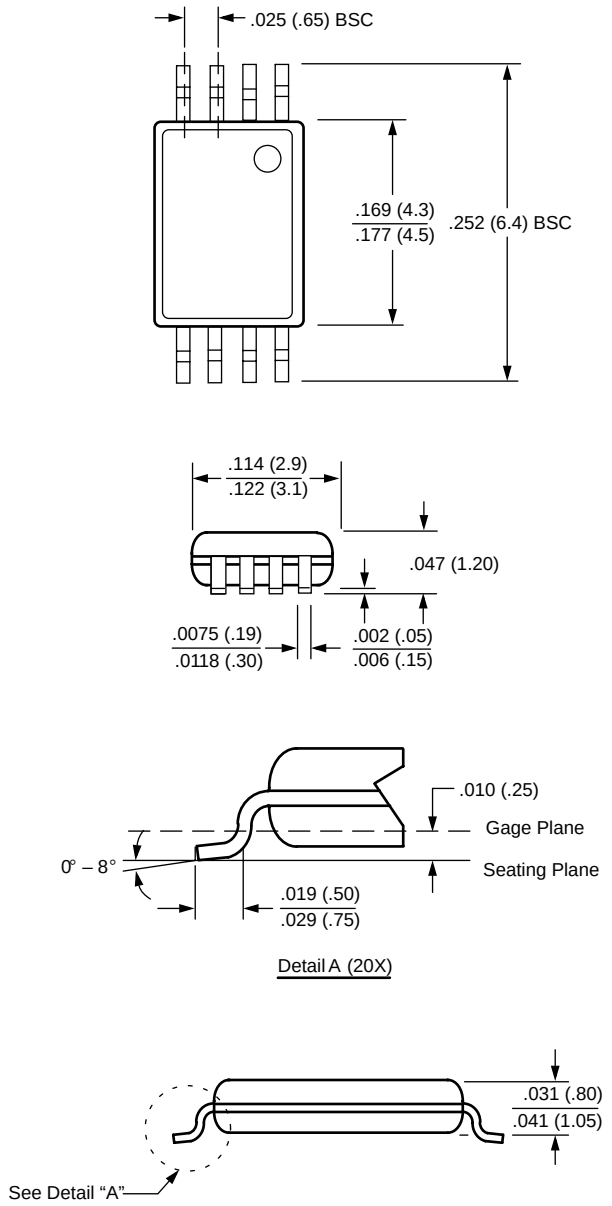
PACKAGING INFORMATION

14-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

8-LEAD PLASTIC, TSSOP, PACKAGE TYPE V



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

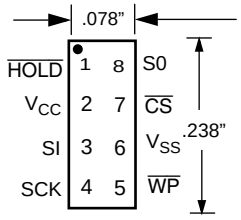
PACKAGING INFORMATION

8-Lead XBGA

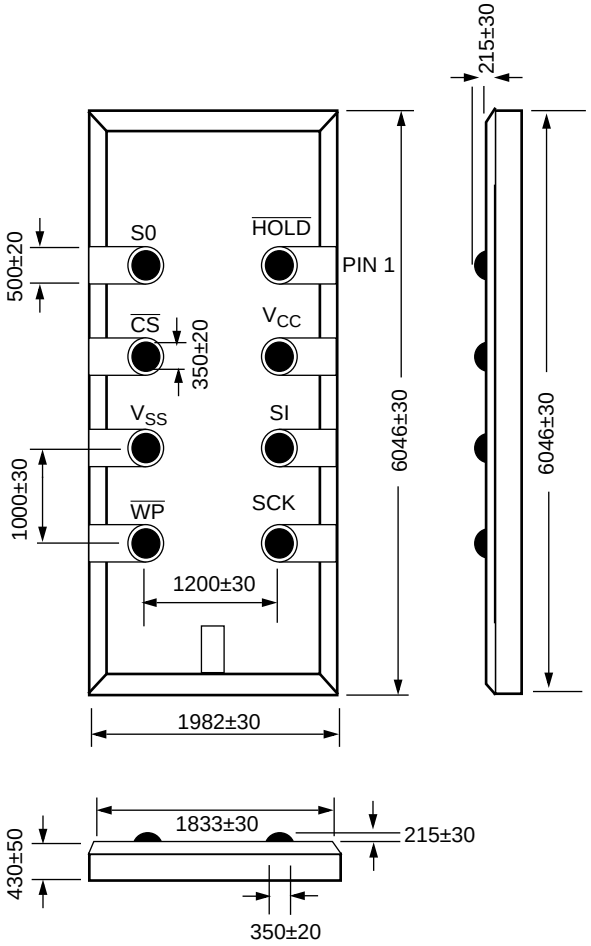
8-Lead XBGA

Complete Part Number	Top Mark
X25138Z-2.5	XAAD
X25138ZI-2.5	XACR

8-Lead XBGA: Top View

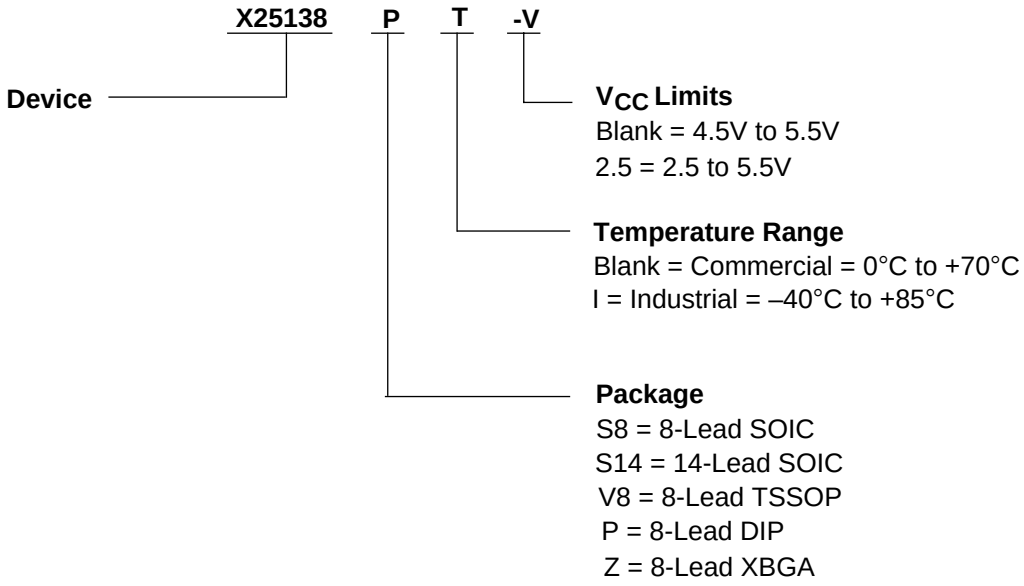


X25138: Bottom View



ALL DIMENSIONS IN μM
ALL DIMENSIONS ARE TYPICAL VALUES

ORDERING INFORMATION



PART MARK CONVENTION

8-Lead TSSOP

EYWW
5138XX

AA = 4.5 to 5.5V, -20 to +85°C
AC = 2.5 to 5.5V, -20 to +85°C
F = 2.5 to 5.5V, 0 to +70°C
G = 2.5 to 5.5V, -40 to +85°C
Blank = 4.5 to 5.5V, 0 to +70°C
I = 4.5 to 5.5V, -40 to +85°C

8-Lead SOIC/PDIP

X5138 X
XX

Blank = 8-Lead SOIC
P = 8-Lead PDIP

AA = 4.5 to 5.5V, -20 to +85°C
AC = 2.5 to 5.5V, -20 to +85°C
F = 2.5 to 5.5V, 0 to +70°C
G = 2.5 to 5.5V, -40 to +85°C
Blank = 4.5 to 5.5V, 0 to +70°C
I = 4.5 to 5.5V, -40 to +85°C

8-Lead XBGA

Complete Part Number	Top Mark
X25138Z-2.5	XAAD
X25138ZI-2.5	XACR

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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